

ABSTRACT SUBMISSION TO:

ISMI Symposium Austin/Denver

1. Title of paper:

“Lithography Cell Productivity Improvement Approaches”

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Abstract

Lithography scanners represent the most cost-intensive tools in a semiconductor manufacturing. To ensure a cost-efficient lithography process, the scanner should always represent the internal bottleneck within a linked lithography cell. Therefore it is specifically important to maximize the scanner performance and their output.

This paper provides an overview of how to increase the productivity of linked lithography cells. Methods and approaches are outlined to guarantee that.

At first an adaptation model summarizes procedures to adjust track and scanner process times per lithography layer and product. It shows which entity is the actual internal bottleneck and what changes have to be made to achieve a well working litho cell.

Occurring cell overhead times are investigated and approaches are pointed out to reduce these time losses. Control chart utilities are used to document and control permanently the cell throughput and observe all realized improvement steps.

All given facts and methods in this paper are based on a recent successfully accomplished improvement project at AMD Fab30 driven by Industrial Engineering. This team has been very successful in pushing the lithography cell output beyond its earlier range.