

Effect and Detection of Sub 80nm Particles on a 130nm Logic Process

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As integrated circuit linewidths and critical dimensions shrink, small particles on the order of 60-100nm that did not impact yield on previous technologies, are becoming a major yield problem on 130nm and smaller technologies.

Detection of these particles can be difficult both from the capability of the inspection tool, and the review on a Scanning Electron Microscope (SEM). Another factor of difficulty in using defect sizes that are atypical in the industry, is that the industry has become numb in believing the reported “size” of the particle from the inspection tool, which is usually a laser scanning tool. Inspecting with a particle “size” that is perceived as being much smaller than the status quo can be a major source of contention and also serve as an impediment to making progress. The final issue is the actual wafer quality itself. Wafers that are riddled with crystalline originated pits (COPs) are not fit for use with extremely sensitive recipes. Interstitial rich (I-rich) silicon has to be used in these cases, and that adds cost to making the defect measurement.

We have found several examples where particles in the range of 60-100nm are causing yield issues on 130nm and smaller process technologies. In some cases, we have had to set the laser scan tools for the bare wafer inspections to their maximum latex sphere equivalent (LSE) detection capability, which is 60nm, to even see these small defects. However, when we review the defects of interest (DOIs) we find defects that are usually larger than 60nm and are typically 80 to 120nm in size per a SEM measurement.

We will discuss the way to setup a laser scan tool recipe to detect DOIs using the concept of signal to noise as opposed to the industry standard latex sphere equivalent method. We will discuss the proper way to devise the defect test to catch the DOIs. Typically the defect test must be setup using the concept of Process Induced Defects Per Wafer Pass (PIDPWP) where the real and exact process and process integration are used to make the bare wafer used as the defect test. Finally we will show an example of where using a “signal to noise” type test set at 60nm LSE found a very critical DOI, and when the DOI was fixed, a major yield improvement was noted.