

## UV scanning enabling advanced SOI defectivity monitoring

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As illustrated by Moore's law, device speed improvement has been ensured by shrinking transistor dimensions generation after generation. Starting with the 130nm node, performance enhancements were sustained by the introduction of new materials. The starting substrate has also been proven to be an integral element of sustaining Moore's law. Significant performance enhancements are offered by SOI or strained silicon. SOI is used in volume production today for high performance microprocessors. Device performance has to be combined with high yield in manufacturing. Monitoring defects using low thresholds is key to manufacturing yield. This paper shows how new generation of inspection system are enabling solution to satisfy the industry metrology requirements for Engineered Substrates.

It has been shown that the reflectivity effects in SOI are the limiting factor to meet the inspection requirements described in the ITRS roadmap for design rules lower than or equal to 130nm. The scattering behavior of defects on SOI structures is then depending on silicon and oxide thicknesses. As large variations are experienced, the only way to implement a robust defectivity monitoring is to generate calibration curves for each product generation and SOI thickness. Using this approach, SOI volume defectivity monitoring is successfully implemented at the 130nm node using current SP1 tools with optimized optical configurations.

KLA-Tencor Surfscan SP2 uses a UV laser resulting in constant reflectivity regardless of SOI thickness for top silicon thicknesses >20nm. To validate this model, calibrated defect sizes were measured for 2 different SOI thicknesses. The scattering behaviour on the different SOI thicknesses is identical. This means that costly calibration curve generation by thickness is no longer needed. When focusing on ultrathin (< 20nm), better scattering behavior can be expected, proving extendability of the new system to several product generations, including future sSOI products as well as fully depleted products.

Similar yields are reported for microprocessor device processing on SOI and bulk. Because of inspection limitations on SOI previously described, it has not been possible to evidence this by inspecting bulk and SOI using same recipe. UV scanner (SP2) allows such comparison with 700/1450 Å XUT Unibond SOI benchmark with epi wafer at 85 nm threshold. They are both showing similar defect level, enforcing yield results equity for both substrates.

Using the SP2, SOI behaves like bare silicon regardless of silicon and oxide layer thicknesses. Very promising early results are confirming simulation and positioning the SP2 as an enabling tool for the whole SOI manufacturing. Aggressive thresholds are demonstrated, closing gaps with industry roadmaps. Complete results will be shown and discussed, including ultra-thin film experiments.