Abstract for: Intentional Defect Arrays for 65nm Technology and Beyond
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There is currently a lack of measured, credible standards for defect detection of particles on patterned wafers in the 65nm technology node. Defects of interest extend to a size of 25% of the design rule.

The International SEMATECH Manufacturing Initiative (ISMI) is seeking to create wafer standards containing Intentional Defect Arrays (IDAs). The design for these IDAs currently incorporates the sizing for process levels found at the 65nm node. To avoid current photolithography limitations, ebeam direct-write lithography is being used to pattern typical logic patterns with intentional defects sized to 25% of the 65nm design rule for each level. These IDA wafers will be used to evaluate detection performance of advanced defect detection equipment.

The IDA design was guided by ISMI and prepared for layout by Benchmark Technologies, Lynnfield, Massachusetts. The design incorporates typical SRAM and logic cells sized from an original 130nm layout. For the 65nm database, only the logic portion of the original design is used in order to avoid excessive write time on the ebeam tools.

There are two basic categories of programmed defects in the design, square (island) and clear (hole).

The eleven different square (island) defects are: center (isolated), bridge-X, bridge-Y, line end extension-X, line end extension-Y, outside corner extension-X, missing, misplacement-X, misplacement-Y, bias (-50% to +200%), and inside corner extension-Y. The center (isolated) defect is a structure with no immediate surrounding structures. The bridge defects form new geometry between unassociated structures in the cell. Line extensions form additional geometry beyond the intended line. Missing defects are geometries removed from the intended structure. Misplacement defects are minimally sized structures that are iteratively moved along an axis toward and away from intended structure. Bias defects are placed near intended structure and are iteratively sized at different proportions of the 65nm design rule.

The three clear (hole) defects are: center intrusion, edge intrusion-X, and line center intrusion. A center intrusion defect is a hole generated from the center of an intended structure. An edge intrusion defect creates a hole starting from the edge of an intended structure. A line center intrusion defect is a specific hole that interrupts an intended structure perpendicularly across the structure's entire width.

Defects are sized across a range from 200% of the 65nm design rule to 25% of the design rule. A cell containing a defect is placed in the center of an array of cells that forms a block of the defective die structure. A defect-containing

die is constructed with 225 blocks (15 x 15). The blocks contain defective cells that decrease in size from 200% to 25% of the design rule as one proceeds in the layout from left to right. Different defect types are found in different rows of blocks as one proceeds from top to bottom.

When non-defective die are alternated with defect-containing die, a typical die-compare structure results that can be utilized by defect detection tools to determine the presence and location of the intended defects.

Initial etched 200mm wafers of these defect standards have been completed by a vendor. Different defect types have been achieved with varying size ranges. Intended sizes are not always achieved, but defects as small as 9nm have been produced, with significant populations below 40nm.