Strategies to prevent yield loss in the next technology nodes

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Yield managers and engineers notice with growing concern the increasing challenges of state-of-the-art yield management practice. While “Systematic Mechanisms Limited Yield” has been identified as a dominating yield limiter, little has been published about how related issues can be methodically tackled. While we expect that the need to deal with systematic yield loss will still increase with the next technology nodes, recent model-based predictions from our research indicate, that in addition defects will gain undesired importance again at 65nm and below.

Fortunately, each state-of-the-art semiconductor fab produces every hour a vast amount of data, in which critical pieces of information and warnings for possible yield loss are often available.

Unfortunately, this critical information is often hidden in the overabundance of these data.

Hence, new statistical methods and analysis techniques are required and will be presented in this paper. These methods have a very high leverage in terms of productivity, as they use only already existing data to create an enormous added value.

We will show new strategies to handle both systematic and defect related yield issues. This includes not only new analysis techniques & algorithms, but also new developed methods for early warnings of yield degradation instead of post-mortem yield analyses.