Stochastic Integration in Design Yield Analysis

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With the advent of the ability to routinely produce process response surfaces of parametric behavior having less than 1% error across the entire design and process window, and timing delay behavior surfaces with error typically less than 100 femtoseconds, the potential now exists for stochastic integration, as applied to surrogate response models, to accurately simulate performance yield metrics previously difficult to evaluate.

For example, yield analysis with 0.5 ppm upper 90% confidence bounds for mild to moderate worst case process drift can be routinely performed for critical device modules such as memory cells.

The methods are simple enough, and CPU resource requirements are low enough, that even simultaneous evaluation of the overlap between Fab wafer disposition criteria and all design performance criteria for individual modules is feasible. With suitable proxies for response variation, one can extend these methods to optimize both for yield and for the alignment of disposition and design criteria.