

## Defects-based Yield Modelling in Semiconductor Manufacturing

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Abstract: The model introduces formulas establishing cause-and-effect connection between observed defects on manufactured chips and their failures. The formulas take into account a number of defect characteristics, such as defect type, size, frequency, and location. The effects of these factors are estimated based on data. The estimation process is complicated by a number of issues, such as a high fraction of uninspected layers and unclassified defects. Results of this analysis are used for yield prediction and for designing optimal yield-enhancement strategies.