

Leveraging Design for Process Technology Evaluation Prior to First Silicon  
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As process technology pushes towards the 65nm and smaller geometries, manufacturing control constraints and device requirements appear to be on a collision course for yield and performance. It is desirable to evaluate the expected yield impact of design and process choices prior to first silicon. In addition, it is also desirable to determine process / design interactions over temperature and voltage, set process window and control targets, and fine tune critical sub-elements of a circuit prior to initial tapeout.

By 1989, Latin Hypercube Monte Carlo and statistical methods originally developed for nuclear weapons yield evaluation were adapted to SPICE simulations by the author to optimize performance of sense amps at one of the major semiconductor manufacturers. This methodology, previously presented at Sematech, proved valuable in that sense amp performance was simultaneously optimized for speed, power, and noise typically within a single day. While it was realized that process technology could be evaluated in a similar manner to improve overall yield, there was little interest at the time in pursuing the methodology for that purpose.

On the other hand, at this particular manufacturer, it was realized that there was value to submitting a large number of SPICE runs at one time during product design. Two additional styles of submissions developed: submitting a grid of changes for particular variables and submitting random changes of those variables. This simplification worked very well when only a few design variables were optimized – it eliminated a need for statistical analysis by simply “picking the winner.”

Since 1989, less efficient traditional Monte Carlo methods have become widely available within the design community. It is now common to work with between 20 and 300 design and process variables -- often 10's of thousands of simulations are performed at one time while yield evaluations sometimes use over 100,000 random simulations.

Due to the large number of design and process variables combined with the presence of more conflicts between performance requirements and process control capabilities, yield and performance optimization are again challenging. It is impossible to submit a dense grid in 20 dimensional space to search for an optimum process window in 8 simultaneous responses using pick the winner strategies. Likewise, evaluating 5-sigma yield performance for even a small number of variables (eg: assessing across-die 6T-cell parametric yield) require literally millions of simulation runs using typical methods.

This presentation reintroduces Latin Hypercube Monte Carlo methods in combination with selected statistical analyses to evaluate process windows, optimize device performance, and evaluate yield efficiently. Using these methods, it is possible to check process windows for a design in hours rather than weeks or months. It is possible to understand design/process sensitivities across the entire process and use window – thus permitting the recommendation of post Fab test screens and Fab process tweaks. It may also be possible to examine interactions between device blocks.