Wafer Probe Roadmap: Guidance for Wafer Probe R&D Resources – 2002 Edition

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Abstract: This document from the Wafer Probe Benchmarking project (MFGM007) provides a wafer probe technology roadmap for 2002 through 2005. It is an update and expansion of Technology Transfer #96073155A TR, *SEMATECH Advanced Probe Technology (APT) Specification*. This roadmap document explains the data and direction of key wafer probing-related parameters compiled from data collected by the six probe project member companies from their internal roadmaps. The roadmap is organized into three sections: Product-Driven Requirements, Wafer Probe Technology Requirements (independent of product type), and Wafer Probe Operations Requirements (selection/procurement/use of probes). The appendix contains an excerpt from the 2001 *International Technology Roadmap for Semiconductors* (ITRS) that summarizes complex and immediate challenges for wafer probing.

Keywords: Benchmarking, Electrical Test, Parametric Test, Probes

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Table of Contents

1 EXECUTIVE SUMMARY 1
  1.1 Roadmap Objectives 1
  1.2 ISMT Wafer Probe Benchmarking Project 1
    1.2.1 Industry Engagement 1
    1.2.2 Data Collection Template 2
  1.3 Roadmap Data Sources and Rollup 2
    1.3.1 Leading-Edge vs. Volume Production 2
  1.4 Roadmap Organization 2
  1.5 Product Family Definitions 3
2 PRODUCT DRIVEN REQUIREMENTS FOR WAFER PROBING 4
  2.1 Introduction 4
3 WAFER PROBE TECHNOLOGY REQUIREMENTS 4
  3.1 Introduction 4
  3.2 Interconnect Deformation 4
  3.3 Multi-Device Under Test 5
  3.4 Electrical Performance 6
  3.5 Thermal Performance 7
4 WAFER PROBE OPERATIONS REQUIREMENTS 8
  4.1 Unit Cost and Cost of Ownership 8
  4.2 Leadtime 8
  4.3 Cleaning 8
APPENDIX A DIFFICULT CHANGES 10
  Introduction 10
  Trends Affecting Probe Card Technologies 10
  Issues and Challenges 10
APPENDIX B GLOSSARY 12

List of Tables

Table 1 I/O Pad Size and Scrub 5
Table 2 Multi-DUT Probing 5
Table 3 Electrical Performance 7
Table 4 Thermal Performance 7
Table 5 Order Leadtime 8
Table 6 Touchdowns Before Cleaning 9
Table 7 Probe Card Difficult Challenges 11

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Company	Representative(s)
Agere Systems	Phil Seitzer
Infineon	Gavin Gibson & Oliver Nagler
International Business Machines	Fred Taber (Probe Project Chair)
Motorola	Bill Williams
Philips	Doug Carlyle
ST Microelectronics	Herve DeShayes

The process of determining the probe roadmap data/information needed, then collecting and preparing it is fully described in the Scope section. This process involved not only the primary representatives and their company colleagues from each of the ISMT Probe Project member companies and ISMT, but also many people from companies and organizations across the wafer probing industry. Without their encouragement, contributions and support this probe roadmap would not have been possible.

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The 2001 Southwest Test Workshop provided a forum for an open industry review and discussion of the proposed roadmap data collection template. Over 50 people attended that meeting, providing valuable insight and direction to the roadmap development team. Thanks go to Bill Mann, Chairman of the Southwest Test Workshop, for graciously providing not only the opportunity to engage his attendees in the roadmap process, but also for providing the meeting facilities.

1 EXECUTIVE SUMMARY

The International SEMATECH (ISMT) Wafer Probe Benchmarking project (MFGM007) was formed in March 2000 to target and drive improvements in wafer probe operations, specifically probe card technology and performance. The project objectives are to enable reliable and cost-effective probing during sort (wafer test).

A number of approaches facilitate accomplishing these objectives:

- Benchmark metrics
- Best-in-class identification
- Best practice sharing
- Site visits
- Networking
- Validation of industry roadmap directions
- Communication of consensus requirements to suppliers
- Sub teams/focus groups on specific topics of interest

1.1 Roadmap Objectives

An ISMT wafer probe roadmap, *SEMATECH Advanced Probe Technology (APT) Specification* (Technology Transfer #96073155A-TR), was published in 1996. See http://www.sematech.org/public/docubase/abstracts/3155atr.htm. This document updates and expands upon that specification.

This wafer probe roadmap document displays and explains the data and direction of key wafer probing-related parameters, as compiled from data collected by the six probe project member companies from their internal roadmaps. The aim is to better understand the challenges wafer probe professionals are facing and provide guidance for development and implementation of advanced wafer probing technologies, techniques, methods, and processes. This document is a kind of collective "requirements statement" on future wafer probing technology needs from leading semiconductor manufacturers.

1.2 ISMT Wafer Probe Benchmarking Project

In 2000, the custom-funded ISMT Wafer Probe Benchmarking project was formed. With its mission to provide industry guidance, in 2001, the project began updating the Wafer Probe Roadmap.

1.2.1 Industry Engagement

To kickoff the update, several representative wafer probe suppliers were asked for feedback on the 1996 roadmap document. This provided an opportunity to align the roadmaps for semiconductor manufacturers' needs with suppliers' solutions. A draft data collection template, illustrations, and glossary were developed and reviewed at an open meeting during the IEEE Southwest Test Workshop in June 2001. Over 50 people from the wafer probe community attended the meeting. Their collected comments shaped the final format and contents of the template.

1.2.2 Data Collection Template

Following the 2001 Southwest Test Workshop, the Probe Project members refined the data collection template, illustrations, and glossary. In September 2001, with the format finalized, data collection began.

1.3 Roadmap Data Sources and Rollup

Much of the raw data from which the tables/graphs in this document are derived come directly from the probe project member companies. Occasionally, excerpts from or reference to the *International Technology Roadmap for Semiconductors* (ITRS) is included.

Each of the Wafer Probe Benchmarking member companies provided data reflecting their company's wafer probing requirements. Each member company entered their data using the data input template noted above. The compilation of the roadmap from each of the individual member company's data into a single rolled-up data point for each parameter was performed by the Probe Benchmarking team and facilitated by ISMT. The rollup algorithm was designed to capture the volume/mainstream production trend(s) of each parameter for each product category across all roadmap outlook years.

1.3.1 Leading-Edge vs. Volume Production

The tables in this document reflect volume/mainstream production data. To derive a leading-edge timing indicator from those tables, a guideline of 12–18 months before volume production is suggested. Note that references to the ITRS capture data reflecting the first year of production. Integrating the Wafer Probe Roadmap into future updates of the ITRS is being considered.

1.4 Roadmap Organization

The Wafer Probe Roadmap is organized into three sections:

- Product-Driven Requirements
- Wafer Probe Technology Requirements (independent of product type)
- Wafer Probe Operations Requirements (selection/procurement/use of probes)

In addition, Appendix A summarizes particularly complex and immediate challenges facing wafer probing. It was prepared by the probe project for the recently ITRS update and is included here for completeness.

Each of the three sections includes tables showing parameter trend data over the roadmap's time horizon that are explained in the text. Each of the semiconductor product family types (see Product Family Definitions) is included in the tables.

- Product-Driven Requirements captures product requirements that drive wafer-probing technology.
- Wafer Probe Technology Requirements identifies wafer probing specific needs that are independent of product drivers.
- Wafer Probe Operations Requirements addresses selecting, ordering, and using wafer-probing technologies.

1.5 Product Family Definitions

Five product families representing the products produced by the probe project member companies are used to segregate the data for each parameter, since the requirements for each family may differ. The five product families are as follows:

- Memory (DRAM)
- Microprocessor
- Application Specific Integrated Circuits (ASICs)
- Radio Frequency (RF)
- Mixed Signal

Memory (DRAM) is the lowest cost and most popular type of semiconductor read/write memory chip; DRAM devices are volatile memories with single-transistor memory cells. Dynamic means the device’s memory cells must be periodically refreshed. Information stored in the memory cells is accessed randomly. Static random access memory (SRAM) devices are excluded.

Microprocessor (MPU/CPU) devices contain the basic arithmetic, logic, and control elements for a computer to process data. “Microprocessor” refers to an integrated circuit that accepts coded instructions, executes the instructions, and delivers signals that describe its internal status. The most common usage is in multi-task computer systems such as PCs. Unlike microcontrollers, microprocessors contain no addressable ROM or RAM. MPUs are subdivided into 8-, 16-, or 32-bit. Similar terms are “processor” and “CPU.”

Application Specific Integrated Circuits (ASIC) devices are designed to suit a customer's particular requirements. The manufacturer assumes wafer design responsibility and may use gate array methodology, a standard cell approach, a unique circuit design, or any combination thereof. These ICs are manufactured using vendor-supplied tools and libraries and are marketed to a single customer. Also included are devices initiated by the manufacturer to fill a perceived need in a given market segment, which the manufacturer lists in catalogs and sells to any customer.

Radio Frequency (RF) refers to integrated circuits operating in the range of electromagnetic frequencies above the audio range and below the visible light. RF ICs are designed specifically for telecommunication, transmission, two-way and cellular radio, data communications, and other communication equipment. Standalone RF products are linear having 100% analog I/Os.

Mixed Signal devices have both digital and analog functions on the same chip, permitting a high degree of system integration. Mixed signal ICs contain analog in more than 50% of the chip area. Mixed signal products include data converter/switch/multiplexer ICs, interface ICs, telecom ICs, and disk drive ICs.

2 PRODUCT DRIVEN REQUIREMENTS FOR WAFER PROBING

2.1 Introduction

Many wafer technology specifications/requirements drive probe technology. Among these are pad/bump pitch, the number of I/Os on the device, metallurgical characteristics, device operating voltages and AC electrical performance. The 2001 edition ITRS is the suggested source to gather this information (see http://public.itrs.net).

In particular, the Executive Summary, Test and Test Equipment, and Assembly and Packaging sections are recommended. The following tables and accompanying text are of particular interest:

- Tables 3a, 4a and 6a in the Executive Summary
- The entire Test and Test Equipment, with a focus on tables 23a, 24a, 25a, 26a, 27a, 28 and 29a
- Tables 77 and 81 in Assembly and Packaging

As noted earlier, including the Wafer Probe Roadmap within future updates of the ITRS is being considered.

3 WAFER PROBE TECHNOLOGY REQUIREMENTS

3.1 Introduction

This section explores the challenges of probe technologies independent of those driven by the devices being probed. These include the resulting behavior of the probe when/after contacting the wafer, the design of the probe card to realize the productivity benefits of probing multiple die at the same time, and the environment within which the probe card is expected to operate.

3.2 Interconnect Deformation

I/O density requirements are driving pad/bump sizes to ever smaller sizes (see Table 1). Though it is well known that on the leading edge, pad pitches are under 50 µm (with resulting pad sizes less than that), the current mainstream still has more “relaxed” pitches. Nonetheless, it is a formidable challenge for probe technologies to continually scale down when this scaling is accompanied by a parallel scaling-down of the permissible probe mark.

Using cantilever probes for probing wirebond technologies, though still a leading solution today, is reaching practical limits in pitch and scrub. Thus newer technologies, perhaps using “semiconductor-like” processes, will be needed.

The increasing application of area array solder bumps brings the commensurate need for vertical probing technologies. Though pitch reductions are foreseen, reductions may be delayed until second-level packaging constraints are resolved. As the pitch/bump dimensions get smaller, current vertical technologies, typically an array of guided wires, may also reach their practical limit, thus requiring newer technologies to be developed.

Table 1 I/O Pad Size and Scrub

Year of Production	2002		2003		2004		2005	
I/O Pad Size (um)	X	Y	X	Y	X	Y	X	Y
Wirebond	50	90	45	80	40	70	35	60
Bump	100	100	75	75	75	75	75	75
Scrub (% of Pad)	Area	Depth	Area	Depth	Area	Depth	Area	Depth
Wirebond	25	90	25	75	25	75	25	50
Bump	30	30	30	30	30	30	30	30

3.3 Multi-Device Under Test

Productivity gains are often realized when testing (probing) more than one device in parallel. In memory testing, for example, it is common to test 32 devices in parallel. As Table 2 indicates, virtually all memory testing is done in multi-device under test (multi-DUT) fashion. The move to multi-DUT testing within other product categories is already underway and accelerating.

Multi-DUT probing requirements drive the need for more and more probe contacts across an ever-growing area. Ultimately contacting the entire wafer will be required; even today, some new contact/probe technologies claim full wafer contact capability or very close to it.

Table 2 Multi-DUT Probing

Year of Production	2002		2003		2004		2005	
Volume (% of Total Wafers Probed)								
Memory (DRAM)		99.9		99.9		99.9		99.9
ASIC		25		33		45		50
Microprocessor		50		60		75		75
RF		20		30		40		45
Mixed Signal		30		40		45		45
Size of Probed Area (mm^2)								
Memory (DRAM)	32 to 128 Devices		64 to 192 devices		64 to 380 devices		100% of wafer	
ASIC		1450		1560		1700		1700
Microprocessor		1450		1560		1700		2050
RF		313		625		625		900
Mixed Signal		513		1063		1225		1413
Number of Probe Points/Touchdown	Signal	Total	Signal	Total	Signal	Total	Signal	Total
Memory (DRAM)	860-3450	1120-4480	1730-5180	2240-6720	1730-10260	2240-13300	14500	18700
ASIC	625	1250	775	1550	950	1900	1050	2100
Microprocessor	260	775	310	925	400	1200	450	1350
RF	125	225	180	325	235	425	250	450
Mixed Signal	250	330	375	500	375	500	450	600

3.4 Electrical Performance

The probe card provides electrical contact between the DUTs on a wafer and the test system electronics. The probe card must faithfully transmit/deliver DUT power and signals from/to the test system.

The wafer probing community expressed interest in roadmap information on four key electrical parameters:

1. Current (max.)
   - At probe tip
   - DC leakage
2. Resistance
   - Contact
   - Series
3. Device Operating Voltages
4. AC Characteristics
   - Bandwidth (test operating frequency)
   - Reflections

The ITRS document is the suggested source for device operating voltages and AC characteristics – bandwidth. AC characteristics – reflections information is not in the ITRS document; data were not available to be collected by the ISMT Wafer Probe Benchmarking Project. However Test and Test Equipment provides tester performance information on a wide range of electrical characteristics that may illuminate requirements for wafer probing.

While the current carrying capability of individual probes contacts (see Table 3) appears sufficient, the aggregate total current across the DUT is expected to rise with growing circuit densities and pin counts. Of note is that some selected applications are seeing the need for higher current carrying capability, approaching 1 amp or more.

Contact resistance is always a closely watched probe technology parameter. It is influenced by many factors (contact force, scrub, cleaning, etc.). The values shown in Table 3 reflect contact resistance under normal usage over the practical lifetime of the probe. Initial and after cleaning requirements are often considerably lower, typically in the 200 milliohm range. Not shown in the table is a growing requirement for lower contact resistance values for longer periods (numbers of touchdowns) before cleaning.

Table 3 Electrical Performance

Year of Production	2002		2003		2004		2005	
Current (Probe Tip Max. mA) (DC Leakage Max. nA)	Probe Tip	DC Leakage	Probe Tip	DC Leakage	Probe Tip	DC Leakage	Probe Tip	DC Leakage
Memory (DRAM)	100	<10	100	<10	100	<10	100	<10
ASIC	300	<10	350	<10	350	<10	350	<10
Microprocessor	350	<10	275	<10	275	<10	275	<10
RF	200	<10	200	<10	200	<10	200	<10
Mixed Signal	250	<10	250	<10	250	<10	250	<10
Resistance (Max. ohm)	Contact	Series	Contact	Series	Contact	Series	Contact	Series
Memory (DRAM)	<1	<4	<1	<4	<1	<4	<1	<4
ASIC	<1	<4	<1	<4	<1	<4	<1	<4
Microprocessor	<1	<3	<1	<3	<1	<3	<1	<3
RF	<1	<2	<1	<2	<1	<2	<1	<2
Mixed Signal	<1	<2	<1	<2	<1	<2	<1	<2

3.5 Thermal Performance

In the timeframe of this roadmap, the wafer probe is expected to see a more demanding thermal environment. In many cases, the low end chuck setpoint is dropping while the high-end setpoint is rising, resulting in a much wider temperature range. This will necessitate selecting materials that handle the extremes and, possibly more notably, dealing with temperature co-efficient of expansion issues.

Table 4 Thermal Performance

Year of Production	2002		2003		2004		2005	
Chuck Set-Point (°C)	Min	Max	Min	Max	Min	Max	Min	Max
Memory (DRAM)	-20	125	-40	140	-40	140	-40	140
ASIC	25	100	25	100	25	110	25	110
Microprocessor	-10	125	-20	125	-30	135	-30	135
RF	25	115	10	120	5	120	5	120
Mixed Signal	25	95	25	115	25	125	25	125
Soak Time (Minutes)								
Memory (DRAM)		10		10		10		10
ASIC		8		8		8		8
Microprocessor		15		13		13		10
RF		10		10		10		10
Mixed Signal		10		10		10		10

4 WAFER PROBE OPERATIONS REQUIREMENTS

4.1 Unit Cost and Cost of Ownership

Probe card unit cost and cost of ownership (COO) trends are not covered in this roadmap. Though individual member companies may have their own approaches to unit cost and COO measurements and goals, consistent models need to be developed that can be used industry wide and that cover the wide range of probe card technologies on the market.

4.2 Leadtime

Driven by the accelerating pace of new design introductions and shrinks, leadtime requirements for initial orders and re-orders are trending downward. Between 2002 and 2005, leadtimes are reduced by nearly 50%. The growing percentage of wafers that are tested in multi-DUT fashion with more complicated probe assemblies magnifies the task of achieving these leadtimes. Strategies, and perhaps technologies, to reduce leadtime are needed.

Table 5 Order Leadtime

Year of Production	2002		2003		2004		2005	
Order Leadtime- Single DUT (weeks)	1st Order	Re-Order	1st Order	Re-Order	1st Order	Re-Order	1st Order	Re-Order
Memory (DRAM)	10	5	8	4	8	4	6	3
ASIC	6	2	4	2	4	2	3	2
Microprocessor	5	2	4	2	4	2	3	2
RF	6	2	5	2	5	2	4	2
Mixed Signal	4	2	3	2	3	2	3	2
Order Leadtime- Multi-DUT (weeks)	1st Order	Re-Order	1st Order	Re-Order	1st Order	Re-Order	1st Order	Re-Order
Memory (DRAM)	11	7	9	6	8	5	7	4
ASIC	9	2	6	2	6	2	4	2
Microprocessor	8	2	6	2	5	2	4	2
RF	8	3	7	3	6	3	5	3
Mixed Signal	6	3	5	2	5	2	4	2

4.3 Cleaning

Generally online cleaning frequency for cantilever probes remains flat; however, probe usage (touchdowns) before offline cleaning is increasing for many of the product families. The goal is better utilization of the test systems and the probe.

For vertical probes, a 50% increase in the number of touchdowns before online cleaning reflects a desire to reduce the vertical technologies' online cleaning frequency to more closely match cantilever technologies. Similar to cantilever technologies, touchdowns before offline cleaning are increasing across all product categories.

While not reflected in the tables, there is a move to eliminate online cleaning for memory products in the later years of the roadmap's horizon. This likely reflects the design and/or

complexity of probes with pin counts approaching full wafer contact. Also not reflected is the growing desire to achieve cleaning-free probing for all products.

Table 6 Touchdowns Before Cleaning

Year of Production	2002		2003		2004		2005	
Touchdowns Before Cleaning (Cantilever)	Online	Offline	Online	Offline	Online	Offline	Online	Offline
Memory (DRAM)	200	6,000	300	15,000	400	20,000	400	20,000
ASIC	3,250	57,500	3,250	57,500	3,250	60,000	3,250	60,000
Microprocessor	1,250	50,000	1,250	50,000	1,250	50,000	1,250	50,000
RF	1,000	100,000	1,000	100,000	1,000	100,000	1,000	100,000
Mixed Signal	2,000	125,000	2,000	150,000	2,000	175,000	2,000	200,000
Touchdowns Before Cleaning (Vertical)	Online	Offline	Online	Offline	Online	Offline	Online	Offline
Memory	1,000	6,000	1,000	15,000	1,500	20,000	1,500	20,000
ASIC	1,000	10,500	1,000	15,000	1,500	17,500	1,500	17,500
Microprocessor	1,000	28,000	1,000	32,500	1,500	35,000	1,500	35,000
RF	100	10,000	100	15,000	100	20,000	100	20,000
Mixed Signal	1,000	55,000	1,000	82,500	1,500	85,000	1,500	85,000

APPENDIX A
DIFFICULT CHANGES

Note: The ISMT Wafer Probe Benchmarking project provided the following section to the 2001 ITRS update.[1] It is repeated here with permission.

Introduction

Wafer probe technologies face complex electrical and mechanical challenges driven by product specifications, test implementation requirements, test productivity goals, and reduced test cost demands. Across the device spectrum, these challenges include: higher frequency response (bandwidth), rising pin counts across tighter pitches and smaller pads/bumps, increasing switching currents (di/dt), alternative pad/bump metallurgies and multiplying test parallelism. Research and development of new or improved probe technologies is required to meet these challenges to ensure that the basic probing requirement of ensuring reliable, sound and cost-effective electrical contact to the DUT(s) is achieved.

Trends Affecting Probe Card Technologies

Along with addressing the key challenges listed below, research and development is urgently required to bring to the market cost-effective probe technologies directed at trends in product offerings and the testing environment.

The continuing volume growth (share of market) of bumped devices, often with I/Os in area arrays, points to the escalating demand for ‘vertical’ style probe card technologies, with a rising need in multi-DUT configurations as well.

Increasingly, manufacturing test of devices is moving to multi-DUT. For some product groups (e.g. memory), current wafer probe technologies handle multi-DUT testing of 32, 64 and even 128 devices in parallel. Probe technologies capable of further increases in parallelism, including up to full wafer (up to 300 mm), are needed to drive test costs lower. For some high I/O count products (e.g. ASICS) multi-DUT probing requirements are emerging.

Wafer probe electrical models, that integrate models of other elements in the path from tester to DUT, will be required of probe suppliers. These models will be needed to conduct simulations of increasingly complex automated test equipment (ATE) to DUT interface networks to optimize performance at the DUT.

As new or advanced probe technologies are entering the marketplace, issues of single-sourcing, order to delivery time, application support and reparability are important and essential considerations in the selection of a probe card for use in volume production.

Issues and Challenges

Table 7 lists other key challenges with specific issues/goals facing wafer probes/probing in the near term.

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[1] Semiconductor Industry Association. *The International Technology Roadmap for Semiconductors*, 2001 edition. International SEMATECH: Austin, TX, 2001.

Table 7 Probe Card Difficult Challenges

Challenge	Issue/Goal
High Frequency Probing	• Traditional probe technologies do not have the necessary electrical bandwidth for higher frequency devices. At the top end are RF devices – requiring up to 40 GHz
Reduced Geometry	• Probe technologies to support peripheral fine pitch probe of 44 µm, and peripheral staggered pad probes at effective pitches of 30/60 • Fine Pitch vertical probe technologies to support 100 µm pitch solder bump and staggered pad devices • Reduction of pad damage at probe commensurate with pad size reductions (or better) • Alternative Probe technology for 3 on 6 mil pitch dense array (vertical probe; bumped device)
Multi-DUT	• Need a probe technology to handle the complexity of "System On a Chip" (SoC) devices at probing of more than one device. • Current Probe technologies have I/O limitations for bumped device probes • Effects on Probes at non-ambient temperatures
Probing at Temperature	• Reduce effects on Probes for non-ambient testing -40 to 150°C; especially for fine-pitch devices
Product	• Probe technologies to direct probe on copper bond pads including various oxidation considerations. • Probe technologies for probing over active circuitry (including flip-chip)
Probe Cleaning	• Development of Inset cleaning mediums/methods, particularly for fine pitch, multi-DUT and non-traditional probes
Cost & Delivery	• Fine pitch or high pin count probe cards are too expensive and take too long to build • Time and cost to repair fine pitch or high pin count probe cards is very high • The time between chip design completion ("tape-out") and the availability of wafers to be probed is less than the time required to design and build a probe card in almost every probe technology except traditional cantilever. • Space transformer lead times are too long, thus causing some vertical probe technologies to have lengthy leadtimes
Probe Metrology	• Tools that support fine pitch probe characterization and pad damage measurements. • Metrology correlation – repair vs. on-floor usage

APPENDIX B
GLOSSARY
(some commonly used wafer probing terms)

Term	Definition
Alignment	Distance from the center of the probe mark to a specified point of probing (not necessarily the middle of the bond pad).
Active Structure Under Pad	Circuitry, including interconnect paths, located directly beneath the bond pad (or bump) used for probing.
Bandwidth	Operating frequency range. Normally, range over which impact on signal is limited to < -3 dB.
Bond Pad	The metal areas on the integrated circuit used for electrical interfacing that the probes contact for testing.
Bond Pad Size/Opening	The measured unpassivated area of the bond pad that can be probed (x, y or dia.).
Bump	Bump or ball of metal deposited on the bond pad for interconnect purposes.
Bump Diameter (µm)	The base diameter of the bump.
Bump Diameter (delta)	The difference in the bump diameter from the original after deformation caused by probing.
Bump Height (µm)	The height of the bump measured from the surface of the bond pad.
Bump Height (delta)	The difference of the bump height from the original after deformation caused by probing.
Bump Metallurgy	Composition of the bump (e.g., Au or Pb%/Sn%).
Bump Volume Displaced	The volume of material displaced by deformation caused by probing.
Capacitive Spec	Capacitive loading of the DUT pin.
Cleaning Frequency	Maximum number of touchdowns by a probe card before cleaning (online or offline) is required.
Cleaning Offline	Cleaning the probe card off the prober (e.g., cleaning station, grinding, etc.).
Cleaning Online	Cleaning the probe card on the prober (e.g., disks, wafers, brush, etc.).
Contact Force	The force applied at overdrive.
Contact Resistance	The effective resistance between probe and bond pad during testing.
Cross Talk	Level of interference between signal lines measured in db.
Current	Current carrying capability of a probe without deterioration of the probe's specified properties. Average, maximum/duty cycle values need to be considered.
Deflection	The distance the probe travels after initial contact with the bond pad relative to the overdrive applied (scrub length/width).
First Touch	When the first probe makes electrical contact with the bond pad.
Inline Pads	An arrangement of bond pads in a single row sharing the same X or Y coordinate.
Leakage	Current leakage with all other pins held to ground.
Matched Impedance	The minimal difference in impedance of signal paths.
Multi-DUT Patterns	The pattern arrangement of the die to allow for multi-DUT probing.
Needle or Pin	A single probe.

Term	Definition
Overdrive Accuracy/Resolution	Capability of the prober to apply additional measured z travel once the probe contacts the bond pad
Pad Damage	Deformation of the bond pad caused by probing (area of disrupted metal/depth into pad/height of disrupted metal above the pad surface).
Pad Metallurgy	The composition of the last (top) metal of the bond pad (e.g., Au or Al or AlSiCu, etc.).
Pad Thickness (µm)	The thickness of the last (top) metal of the bond pad (e.g., Au or Al or AlSiCu, etc.).
Pad Volume Displaced	The volume of material displaced by deformation caused by probing.
Planarity	The vertical distance between the highest and lowest probes on a probe card.
Probe Pitch	The minimum distance between probed points (pads) on a chip.
Probe Scrub Area	The measured area of deformation caused by probing.
Probe Scrub Depth	The measured penetration of the probe mark into the bond pad metal.
Probed Points	The total number of pads or bumps to be probed (signal + power & ground).
Reprobe (max.)	The maximum allowable number of touchdowns on a pad, including those touchdowns (although no testing occurs) due to prober stepping pattern during multi-DUT testing.
Resistance Series/Path (SPR)	The total resistance between the tester and probe, including interconnects, PCB, components, fixed probe resistance, etc.
Signal Matching	Minimizing the difference in impact on signals by using matched impedance.
Staggered Pads	Multiple closely spaced parallel rows of pads with an offset in x or y or pitch between rows.
Tier/Layer	One epoxy layer/ring of probes. Multiple tiers may be used for "outreach" probes.
UBM	Under bump metallurgy; used to enhance bump adhesion to the bond pad.
XY Area	Total x,y dimensions to be probed per touchdown. Single DUT = chip x,y dimensions. Multi-DUT = chip x,y dimension times # DUTs x,y plus # of x,y scribe linewidths

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