Call for Improved Electromigration Simulation Tool

International SEMATECH
Technology Transfer #01084148A-XFR

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Abstract: This paper is intended to help the semiconductor industry develop and communicate a consensus position for suppliers for improved electromigration electronic design automation (EDA) tools. The statement of needs includes tool input, outputs, features, and performance capabilities.

Keywords: Suppliers, Supplier Relations, Automation, Electromigration

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Table of Contents

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1 EXECUTIVE SUMMARY

This paper has been developed to help the semiconductor industry, as represented by the International SEMATECH member companies, develop and communicate a consensus position on an important need for improved electronic design automation tools for simulating electromigration effects. The shortcomings of current commercially available tools are described and the needs for an improved tool are described in terms of inputs, outputs, features, capabilities, and performance.

It is hoped that suppliers of electronic design automation (EDA) tools in particular will benefit from the assessment contained in this publication.

2 ELECTROMIGRATION DESCRIPTION

As circuit density continues to increase and linewidths continue to shrink, interconnects are increasingly important in setting not only the device performance, but also the overall device reliability. Electromigration, which results from the momenta exchange between current carrying electrons and the host metal lattice, may produce voids in the metallization or increased stress in the supporting dielectrics. Voids will result in increased line resistance or even opens, while increased mechanical stress may result in dielectric fractures and leakage between adjacent interconnects. Products become increasingly susceptible to both of these effects as the interconnect line width and space decrease and line lengths increase. Furthermore, the increasing influence of interconnects resistance-capacitance (RC) delays on overall circuit performance make products more sensitive to these effects.

The rate of electromigration is primarily dependent upon the current density and line temperature following the generally accepted Black model:

$$TF = A_0 (J - J_{crit})^{-N} \exp(E_a/kT),$$

Where: TF = Time to failure

A_0 = Constant related to material and process conditions

J = Current density

J_{crit} = Critical (threshold) current density necessary to produce failure

E_a = Thermal activation energy

K = Boltzman's Constant

T = Line temperature

Generally, both the average current density (J) and average temperature (T) are increasing as the semiconductor technology advances. Consequently, more precise EDA tools that are able to account for the thermal effects are required to design-in reliability.

3 SEMICONDUCTOR INDUSTRY NEED

There is an increasing urgency in the semiconductor industry to be able to accurately simulate the current density and temperature of interconnects in order to prevent electromigration induce failures. Current electromigration and infrared (IR) drop tools do not handle the temperature effects well as the current density and line temperature are interdependent. Not taking into account the temperature during simulation leads to conservative checking and over-design; or worse, underestimates the risks of enhanced electromigration due to increased local temperature. Tools are needed which are able to compute the current densities and local temperature in local interconnects as well as the power grid.

4 MEMBER CONSENSUS OF THE REQUIREMENTS FOR AN IMPROVED ELECTROMIGRATION SIMULATION TOOL

The International SEMATECH Design-in Reliability Team has identified a consensus set of requirements for an improved tool. These requirements are presented here to encourage and facilitate the EDA developers to produce an improved tool or add these new capabilities to their products. This is not a request for quotation.

4.1 Inputs

- Netlist (DEF format)
- Input simulation test patterns and realistic worst-case handling such as upper-bound power-density treatment
- Physical layout (GDS2 format)
- Technology electrical data (parameters for devices and parasitics)
- Width-dependent cross-sectional area measurements
- Technology thermal data (parameters for interconnect and substrate)
- Thickness and thermal conductivity of interlayer dielectric and passivation films
- Technology electromigration limits (more than just current density setting)
- Barrier metal properties
- Package/heatsink thermal resistance model
- Substrate temperature distribution
- Wire bond diagram, bonding type and wire material/size (for Power devices)

4.2 Outputs

- Graphical representation of current densities (J_{AVG} or J_{RMS}) super-imposed on power grid physical layout
- Graphical representation of local temperature super-imposed on power grid physical layout
- Graphical display of device junction temperature with local interconnect temperature along the power grid
- Ability to selectively display lines or list nets that exceed a user specified current density and/or line temperature

4.3 Features/User Interface

- Flagging of power grid elements that violate electromigration limits
- Computation of electromigration risk for other power grid elements
- Possibility to easily run engineering change orders (ECOs) by updating physical layout interactively
- Possibility to compare current densities with and without thermal correction

4.4 Capabilities/Performance

- Ability to process circuits of more than 10 million transistors with run time of several hours on an "average" workstation
- DC (static) and AC (dynamic) analysis

5 RISK OF NOT HAVING TOOL

- Unacceptable product reliability risk if worse-case current density and local temperature effects are not comprehended
- Uncompetitive "over-designed" products if only worse case, non-temperature corrected simulations are used that won't occur on silicon because of the resulting local heating that will reduce the actual current densities.

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