



**Use Condition Based Reliability Evaluation: An Example
Applied to Ball Grid Array (BGA) Packages**

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Use Condition Based Reliability Evaluation: An Example Applied to Ball Grid Array (BGA) Packages

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Abstract: Increased package performance expectations, new packaging materials, and market segmentation are key trends in today's semiconductor industry. The SEMATECH Reliability Technology Advisory Board has developed a reliability test methodology to keep pace with these market trends. Based on that methodology, the SEMATECH Qualification, Monitors and Controls Team has produced this paper, which provides an example of how to apply the method to ball grid array (BGA) packages. An example of the use conditions qualification methodology is presented in detail. The methodology is briefly defined and input requirements are listed. Accelerated test conditions are developed, based on knowledge of the customers' use conditions, activation energies, and failure models. Test conditions that produce statistically justifiable failure populations that are not likely to occur in the defined use environments are minimized or eliminated. Examples of legacy test conditions from several companies are provided for comparison.

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EXECUTIVE SUMMARY

Increased package performance expectations, new packaging materials and market segmentation are key trends in today's semiconductor industry. The SEMATECH Reliability Technology Advisory Board has developed a reliability test methodology to keep pace with these market trends. The Use Condition methodology provides for selecting stress conditions based on knowledge of the components usage environment. Based on that methodology, the SEMATECH Qualification, Monitors and Controls Team has produced this paper which is an example of how to apply the method to BGA packages. Compared to stress-based methods, this approach requires more knowledge about the physics of failure mechanisms and about the anticipated use of the component.

ABSTRACT

An example of the Use Conditions Qualification methodology is developed and presented in detail. The methodology is briefly defined and input requirements are listed. Accelerated test conditions are developed based on knowledge of the customers' use conditions, activation energies and failure models. Test conditions that produce statistically justifiable failure populations that are not likely to occur in the defined use environments are minimized or eliminated. Examples of legacy test conditions from several companies are provided for comparison.

1. INTRODUCTION

Through a detailed comparison of qualification practices, it was determined that companies are using different procedures and tests to qualify similar package technologies. Package subcontractors, IC manufacturers and the final customer will sometimes perform their own qualification on a new package technology delaying the introduction of this package into final use. It was determined that there was a need to come up with a uniform qualification methodology that could be used with these new package technologies.

In trying to come up with a uniform set of qualification tests/requirements, it was determined that the use conditions of the package would be very important in determining the qualification tests that should be performed. There is such a wide range of possible use conditions that the approach of trying to establish even a minimum set of qualification requirements that would apply to all applications was abandoned. It was decided that a better way to handle this problem would be to determine a methodology that would establish the qualification testing that is based on the actual use conditions of the package

The purpose of this paper is therefore to serve as an example of using the RTAB "Use Condition Based Reliability Evaluation of New Semiconductor Technologies" methodology to determine the use conditions for BGA packages and then to establish the stress requirements necessary to qualify the package for the intended use. This paper will serve only as an example of how this methodology should be performed. It is not intended to be considered as a specification. Every company that desires to use this methodology will have to determine the failure mechanisms, activation energies and other information that is specific to their own package.

Each company that makes use of this methodology will also have to determine whether to perform the necessary testing using test chips and/or actual product. For the purpose of this example paper, the demonstrated procedures would be the same if either test chips or actual product were used.

2. DESCRIPTION OF RTAB METHODOLOGY

This section is a brief description of the RTAB Use Conditions Methodology.

A. Definition of Environmental, Lifetime and Manufacturing Conditions

Define the environmental, lifetime and manufacturing conditions the package will be exposed to. The criteria that need to be considered for the intended application include:

- the expected operating lifetime of the package
- the actual number of weekly operating hours
- the number of environmental and power cycles experienced per day
- the relative humidity and temperature of the operating environment
- the overall storage temperature
- the cumulative end of life failure rate

B. Determination of Exploratory Reliability Stresses

Determine an initial set of reliability stresses to be used for collecting data on failure mechanisms. These stresses must be chosen so as not to exceed the physical capability of any of the materials used in the package. It is assumed that the use conditions are within the physical capability of the package material set. A list of commonly used stresses is included in the RTAB document. It is necessary to determine if there is anything unique about the package that may require new or modified stress tests. It is also necessary to determine:

- the appropriate models to be used
- possible failure mechanisms
- acceleration factors for each failure mechanism

All of the above factors can then be combined to determine the initial set of stresses. As noted in the RTAB paper, a number of these factors may be known based on historical data.

As in the RTAB paper, this step should be divided into a number of interrelated activities. For this paper these activities have been applied to BGA packages and will be discussed in detail in Section 5.

C. Determine Extended Stress Conditions

Define extended stress conditions based on the estimated acceleration factors. The purpose of the extended stress conditions is to help define the margin of the technology, identify all of the possible failure mechanisms and to determine the actual acceleration factors.

D. Apply Data to Models

Perform testing using the initial and extended stress qualification conditions. The actual test results can then be compared to the results predicted by the models to determine if the technology follows the model or follows a new acceleration curve. Acceleration factors may have to be recalculated at this point.

E. Determine Final Reliability Stress Conditions

The next step is to use the acceleration factors determined above to come up with a final set of qualification stress conditions and duration. It is important to look for and discount irrelevant failure mechanisms.

F. Establish Baseline Performance

Establish a baseline performance for the material set or process that is being qualified.

3. COMPARISON OF QUALIFICATION METHODOLOGIES

The following chart briefly compares the traditional, "Legacy", qualification method and "Use Condition" method, summarizing advantages, disadvantages and information required.

Comparison of Benefits and Data Requirements “Legacy” vs. “Use Condition” Qualification Methodologies

Legacy (Traditional) Based Qualification	“Use Condition” based Qualification
<ul style="list-style-type: none"> • Certification requirements based on standard stresses • Stress technology is fixed and doesn't easily accommodate new requirements • Reviews are done only in response to extremely significant changes • New technologies must meet requirements far beyond their useful life. • Advantage: simplicity in collecting and reporting data • Disadvantage: Limited understanding of package performance Limited knowledge of application failure rates • Internal Supplier Data Requirements: Attribute data at end points of required stresses 	<ul style="list-style-type: none"> • Certification requirements based on product lifetime • Stress technology scales to match the operating requirement environment of the technology • Automatic review cycle of methods, testing, environment every generation • Allows for optimization of materials and processes for reduced cost • Advantage: More accurate prediction of lifetime performance and margins • Disadvantage: More complex approach for collecting and reporting data • Internal Supplier Data Requirements: Use conditions and lifetime requirements Appropriate attribute and variables data Package materials properties Failure mechanisms associated with each stress Acceleration factors and models for each failure mechanism

4. DATA APPLICATION TO DERIVE ACTIVATION ENERGIES AND FAILURE MECHANISM METHODOLOGY

Definition of Environmental, Lifetime and Manufacturing Conditions

For the purposes of this example white paper the following set of use conditions were selected. These values were selected to illustrate the methodology and are based on a combination of survey data, member company inputs, and judgments by the authors. It will be necessary for each company following this procedure to determine their own use conditions at this step. The data in this and subsequent steps is included only to serve as an example.

Assumptions:

- Operating life: 7 years (62,000 hours = 7 years)
- Power on (hours per week): 168 hours(62,000 hours)
- Power cycles per day: 3 (7500 cycles = 3 X 365 X 7)
- Environmental (ambient temperature) cycles per day: 1 (3000 cycles = 1 X 365 X 7)
- Moisture: 30°C and 85% relative humidity
- Operating temperature range of ambient: 5°C – 45°C ($\Delta T = 40^\circ\text{C}$)
- Storage temperature: -40°C to 55°C
- Maximum junction temperature (T_{jmax}): 100°C
- Manufacturing conditions/considerations: surface mount by convection reflow; JEDEC preconditioning; not exposed to full immersion solder wave

5. DETERMINATION OF EXPLORATORY RELIABILITY STRESSES

The SEMATECH QMC Committee discussed the potential failure mechanisms typically related to BGA packages. As in the RTAB white paper procedure, the QMC group of experts established the list of reliability concerns for the new BGA package. The following is the comprehensive list of failure mechanisms thought possible for the full range of BGA package types currently available.

i. Thermal Mechanical Failure Mechanisms:

CTE Mismatch Device to Package

- Flip Chip(Bumped)/Joint Fatigue of unencapsulated and encapsulated joints
- Flip Chip/Joint Fatigue if delamination of underfill occurs
- Wire Bond Device to Die Attach Adhesive

CTE Mismatch Module to PWB

- BGA Solder Joint Fatigue

CTE Mismatch Encapsulant to Device

- Underfill to Flip Chip Joints
- Overmold/glob top to ILB (Inner Lead Bond)/OLB (Outer Lead Bond)
- Overmold/Glob top to Wire Bonds

Delamination and Loss of Adhesion at Interfaces

- Device to Underfill
- Underfill to Substrate
- Solder mask to Substrate
- Cap/Stiffener to Adhesive
- Overmold or Glob to Device
- Overmold or Glob to Substrate/Tape
- Heat Sink to Cap to Stiffener Interfaces
- Pad adhesion to Substrate

Solder Creep Rupture

- Assembled Module with Large Heat Sink with time and gravity

Metal Circuit Fatigue

- Substrate Circuit Lines
- Inner Lead Bond(ILB)/Outer Lead Bond(OLB)
- Substrate PTHs (Plated Thru Holes)/Thru Vias

Assembly Induced Problems

- Initial Reflow
- Rework
 - BGA Joint Defects, Cu dissolution of pads/circuitry

Defect Failures

- Wire bond Defects (wire nicks, bond foot, etc.)
- Non-uniform joints (higher temperature flip chip joints)
- Non-uniform balls (eutectic solder on BGAs)
- Circuit Lines (neckdowns, mouse bites)
- PTHs (plating uniformity within hole and on the surface)
- ILB/OLB Defects (nicks, etc.)

Device Cracking

- Defects
- CTE Mismatch

Passivation/Thin Film Cracking

- Interaction of Device Passivation and Overmold/Encapsulant

ii. Temperature/Humidity (with and without bias) Failure Mechanisms:

Corrosion

- Oxidation
- Contamination

Metal Migration

- Dendrite Growth
- Corrosion Product Growth
- Metal Depletion into Solution

Oxidation

- Oxide Film Growth

Delamination of Material Interface

- Loss of Interfacial Adhesion

iii. Thermal Aging Failure Mechanisms:

Material Breakdown

- Material Oxidation
- Electrical Degradation
- Thermal Degradation
- Intermetallic Degradation

PROCEDURE:

A. Bound Reliability Stress Conditions Based on Package Material Properties and Capabilities:

Stress conditions must be selected such that the testing does not produce false failure mechanisms that are artifacts of the test conditions and not representative of the product's use environment. For the BGA packages the areas of stress typically used are thermal cycle, temperature/humidity with and without bias and thermal aging. The areas of concern for each stress type are discussed below.

i. Selection of Thermal Cycle Test Conditions

Thermal cycle test conditions, in particular, must be selected with care. The selection of the thermal cycle range and duration for product test should be based on use environment, the life of the product and the material capabilities.

In either development or qualification, several thermal cycle conditions can be performed on the BGA product. Ideally parts should be stressed to a preselected failure percentage. Failure mechanisms should be compared between thermal cycle conditions. It is critical that all failure mechanisms encountered be judged against use conditions for the intended product. Failures that are observed at the most severe conditions may not represent a field concern for that application and are merely an artifact of the severe test conditions. Areas of concerns generated by extreme thermal cycling include exceeding the material's glass transition at high temperature, moisture absorption by the BGA substrate and material ductility at low temperatures. It should be noted that PBGA and TBGA packages, with the organic materials used in these BGA substrates, are more sensitive to some aspects of thermal cycling than CBGA packages. Exceeding the glass transition temperature (T_g) of a material changes the coefficient of thermal expansion as well as the properties of the given material. Exceeding the ductility of materials can generate unrealistic failures due to brittleness and crack propagation at the lower temperature exposures.

ii. Selection of Temperature/Humidity (with and without bias) Stress Conditions

The selection of Temperature and Humidity test conditions must be done with care. Tests such as HAST, autoclave and 85°C/85%RH testing, while being useful development tools, must be used with caution since the stress conditions selected and the duration of the test can cause degradation of package materials which will lead to unrealistic failure of the package with respect to the application environment. It is advisable, when performing T&H testing, that one be able to bridge back to a known T&H condition where the failure mechanisms are known and relate to the field exposure expected for the specific application.

- Excessive package delamination inconsistent with field application conditions.
- Excessive corrosion and metal migration inconsistent with field environment.
- Temperature and humidity effects which one will simply not see in the field application. It is possible that the field application may result in the module operating in a "dry environment" which is being over accelerated by the THB stress conditions.

iii. Selection of Thermal Aging Stress Conditions

The cautions related to this stress condition are exceeding the material T_g and material interface adhesion. Extended exposure of organic BGA packages to high temperatures result in oxidation and breakdown of the organic materials and can adversely affect mechanical and electrical performance of the package.

B. Determine Stresses for Accelerated Testing:

Based on historical data and industry experience with BGA packages, TABLE A was constructed. It shows many possible failure mechanisms and the associated stress tests used to discover concerns.

**TABLE A
Stress Test versus Failure Mechanism of Interest**

TEST/FAILURE MECHANISM	Thermal Cycle*	Power Cycle	Unbiased T&H*	Biased T&H*	Thermal Age
CTE DEVICE TO PACKAGE	X	X			
CTE MODULE TO PWB	X	X			
CTE ENCAP. TO PACKAGE	X	X			
DELAM/LOSS OF ADHESION	X	X	X	X	
SOLDER CREEP RUPTURE	X				
METAL CIRCUIT FATIGUE	X	X			
ASSEMBLY INDUCED	X				
DEFECT FAILURES	X	X			
DEVICE CRACKING	X	X			
PASSIVATION/ THIN FILM CRACKING	X	X			
CORROSION			X	X	
METAL MIGRATION				X	
OXIDATION				X	
THERMAL EFFECTS					X

* Precondition per JEDEC JESD22-A113.

Typical thermal cycle ranges used in test are listed below. In reality, the cycle range and duration selection should be based on the intended use for the BGA package and the failure mechanism of interest. Table A has listed a number of failure mechanisms which, dependent on the application, may require that several thermal cycle test ranges be used to isolate the particular mechanism of interest, while not obtaining tests artifacts that confound interpretation of the data. The ranges listed below are for reference and demonstrate the wide range of thermal cycles that can be used for PBGA testing. A prime example of the need for different thermal cycle test conditions is testing the PBGA module versus testing an assembly with the PBGA module attached. Often the assembly requires a thermal cycle range that the printed wiring

board portion of the assembly can withstand. If too severe a range is selected, the plated thru holes can crack impeding ones ability to test fatigue of the BGA solder joints.

- 0°C to 100°C
- 0°C to 125°C
- -40°C to 65°C
- -40°C to 115°C
- -40°C to 125°C
- -40°C to 150°C
- -55°C to 125°C
- -65°C to 150°C

Other stress tests, such as High Temperature Operational Life (HTOL), while being useful for determining semiconductor failure susceptibility, have not been found to drive any unique failure mechanisms in BGA packages. It is important to look at the failure mechanisms of interest in the BGA package being tested and decide what stress test methodology is best suited for discovering package failure potential.

C. Determine Unique Requirements:

For the PBGA package of interest, most requirements are standard. Unique requirements would be those associated with the assembly of that package to a Printed Wiring Board (PWB). The PWB properties (such as CTE and stiffness), SMT assembly parameters and application layout all can play a role in the reliability performance of the BGA package.

D. Develop or Determine Stress Models for BGA Package:

i. Mechanisms That Have Known Models

Model development includes both stress test based and computer generated information. In particular, finite element modeling, when fine-tuned with stress test data, is very good at identifying regions of high stress for the BGA package. Such models are especially useful for use in follow-on technologies where the database has already been verified with stress test results.

From experience on PBGA packages, it has been shown that flip chip and BGA solder joints, assuming that they are eutectic or 90/10 solder, follow the Modified Coffin-Manson equation described in the next section of this paper. It is important that the thermal cycle regime used employs slow cycling, on the order of 1.7 to 3 cycles per hour (typically 2 cycles per hour) and a dwell of 4 to 5 minutes around the peak temperature. Often a single zone chamber is preferred to maintain the slower ramp rates. The dwell is needed to allow the solder joints to creep. Lack of dwell prevents the normal solder creep and allows the package to perform better in test than in actual use. In order to test the BGA joint integrity, assembly to a PWB is needed. Where applicable, this assembly should simulate the end use with respect to component layout and PWB cross section, in particular. Power cycling has also been established as a method to test BGA integrity. Solder creep rupture requires similar stress conditions. The package requires assembly to a PWB and the attachment of a heat sink. Testing should be performed with the part situated, as it would be in the field.

Modeling and experience have shown that substrate metal circuit fatigue is not susceptible to cycle frequency. However, the type of thermal cycling chosen should be based on the failure mechanism of interest. Wet Thermal Shock is typically used to identify embrittlement and material defect concerns while standard temperature cycling is used to detect low cycle fatigue concerns.

Device defects, such as chip cracking, can be discovered with only a few cycles of thermal cycling. This is because the device is brittle and only a few cycles are needed to activate and extend the crack.

ii. Mechanisms That do not Have Known Models

The following paragraphs cover what can be done for the case of failure mechanisms that do not have known models to describe them.

Passivation/Thin Film Cracking is not typically a BGA package concern. If there is reason to have this concern, it can be identified at low temperature and is the result of adverse interaction between the device passivation and it's over mold/encapsulant.

Delamination is usually moisture driven where temperature and humidity testing is used to discover problems. However, there are cases where it is driven by thermal cycling instead. Straight thermal cycle testing, including JEDEC preconditioning of choice, is adequate to observe this delamination.

The failure mechanisms of interest in temperature and humidity stress are primarily related to material degradation. They fall into three major areas; corrosion, metal migration and delamination of material interfaces.

Corrosion mechanisms fall into two major categories: galvanic and electrolytic accelerated mechanisms. Both can be accelerated by temperature and high relative humidity. Both can be observed under field application conditions.

The metal migration mechanism involves the physical movement of metal atoms from their original location to another, deleterious position. This mechanism involves dissolution and/or transport of metal ions, i.e. dendritic growth, corrosion product growth on the metal or metal depletion into solution with no subsequent deposition on the structure of interest.

Oxidation is defined as the classical mechanism where the electronic state of the metal is changed. The oxidation normally involves growth of an oxide film, which will affect electronic/thermal conduction of the metal film.

Delamination of material interfaces has a critical RH level which will cause water molecules to interfere with material interface bonding, i.e. hydrogen bonding.

T&H stress conditions (with and without bias) of 85°C/85RH are recommended for determination of new failure mechanisms. However, one can proceed with accelerated T&H testing, such as HAST, for the first verification test. If new or unexplained failure mechanisms arise during that test sequence, a validation of the failure mechanism should be performed. One possible method for doing this would be using a T&H test condition for which an extensive database already exists, typically 85°C/85% RH. This test condition has several attributes that make it very attractive for new package and material evaluations. The temperature is comfortably below the Tg of most organic packaging material and the humidity is above the 70% threshold (determined several years ago by empirical data). These conditions seem to activate corrosion and oxidation mechanisms in the T&H environment through the formation of a thin film of moisture on the sample's surface.

From a BGA package evaluation perspective, use of either high or low temperature storage testing has to be based on application requirements. Typically low temperature storage is used when the application is intended to survive long periods at low temperatures. Conversely high temperature storage is used for simulation of burn-in effects, extended operation at elevated temperatures (under auto hood applications) or for accelerating the effects of extended storage at elevated temperature.

E. Technology Failure Mechanisms and Known Acceleration Models:

Based on the expert input obtained from the QMC group and our present base knowledge of failure mechanisms and acceleration factors, the following acceleration models were deemed applicable to the PBGA package in question. Reference RTAB Paper on Acceleration Factors, Models & Reliability Statistics and EIA/JEP122 "Failure Mechanisms and Models for Silicon Semiconductor Devices"

i. Thermal Cycle Failure Mechanisms

The Model suggested in the RTAB Paper is the Coffin-Manson model:

$$N_f = C_0 * (DT)^n$$

The Acceleration factor (AF) is:

$$AF = \frac{C_0 \frac{DT_{stress}}{DT_{use}}}{C_0} = \left(\frac{DT_{stress}}{DT_{use}} \right)^n$$

Where:

N_f = Number of cycles to failure,

C_0 = a material dependent constant,

ΔT = entire temperature cycle-range for the device,

n = an empirically determined constant.

The acceleration factor (AF) is the ratio of $N_{f(USE)}/N_{f(STRESS)}$.

For **Substrate Metal Fatigue** the exponent of 2 is typically utilized based upon historical databases.

For **passivation/thin film cracking** the same equation is used as for metal circuit line fatigue, but the exponent utilized is typically 4.0, but can range from 2 to 11 based on the device passivation used. It should be noted that passivation/thin film cracking on the device is not a typical failure mechanism driven by the BGA package.

With respect to thermal cycle induce delamination there is no known acceleration model.

The Coffin-Manson Model was modified by Landzberg and Norris (1969) to the form:

$$N_f = A_0 * f^\beta * \left(\frac{\Delta T}{DT} \right)^n * G(T_{max})$$

Where:

N_f = Number of cycles to a given percent failure

A_0 = Material dependent constant

f = Cycling frequency

ΔT = Temperature range

G = Arrhenius factor that depends on maximum temperature reached in a cycle (T_{max})

n = An empirically determined constant

β = 1/3

Historical data has demonstrated that we can determine the thermal cycle acceleration (AF) of **solder joint** failures in the BGA package, using the Landzberg and Norris equation above and taking the ratio of $N_{f(USE)}/N_{f(STRESS)}$.

$$AF = \frac{aDT_{stress}^{1.9}}{aDT_{use}^{1.9}} \frac{F_{use}^{1/3}}{F_{stress}^{1/3}} e^{\frac{Ea}{k} \left(\frac{1}{T_{use}} - \frac{1}{T_{stress}} \right)}$$

The strain component is 1.9 for either eutectic or 90/10 solder.

The exponent for frequency is 1/3 and we assume F(USE) is 6. F(STRESS) is usually 48 which equates to 2 cycles per hour. This allows for appropriate time for solder creep to occur during the stress cycle.

ii. Temperature, Humidity and Bias Failure Mechanisms

The model given below was suggested in the RTAB paper and assumes that the bias voltage is constant between use and stress conditions.

$$TF = A_0 (RH)^N e^{\frac{Ea}{kT}}$$

AF = the ratio of TF_{USE}/TF_{STRESS} .

$$AF = \frac{RH_{stress}^N}{RH_{use}^N} * e^{\frac{Ea}{k} \left(\frac{1}{T_{use}} - \frac{1}{T_{stress}} \right)}$$

Where:

A_0 = Material dependent constant

RH = Relative Humidity of Test

N = An empirically determined constant

T = Temperature Degrees Kelvin

k = Boltzmann's constant (8.625×10^{-5} ev/°K)

It should be noted that if the RH is constant between the use and stress conditions the RH term in the AF model drops out and only the thermal portion is left.

iii. Thermal Effects

The model suggested in Reference (RTAB Paper) is:

$$TF = A_0 e^{\frac{Ea}{kT}} \quad \text{and} \quad AF = e^{\frac{Ea}{k} \left(\frac{1}{T_{use}} - \frac{1}{T_{stress}} \right)}$$

Where:

A_0 = Arbitrary scale factor

Ea = Activation energy for the mechanism

k = Boltzmann's constant (8.625×10^{-5} ev/°K)

T = Temperature in degrees Kelvin

F. Section of Qualification Conditions Based on Environment & Models

Table B describes the failure mechanisms found from historical data and during the development/characterization of BGA packages. It gives the environmental stresses used and the associated activation energy or Coffin-Manson exponent found. This information is then used in the appropriate models described in section 5E to determine the appropriate qualification stress conditions and durations.

Table B
Failure Mechanisms with Activation Energy or Coffin-Manson exponent Found during BGA Development/Characterization

Failure Mechanism	Preconditioning	Temperature Cycle Coffin-Manson exp.	Power Cycle	Biased T&H Activation Energy Ea	Thermal Aging Activation Energy Ea
Interface Delamination	No Acceleration		No acceleration		
Substrate dielectric cracking	No Acceleration	1.25			
Substrate Barrel Crack	No Acceleration	2.2			
Intermetallic					1.41
Metal Migration				0.91	
Thin Film Cracking	No Acceleration	3	No acceleration		
Corrosion				0.75	

Table C relates the “Use Environment”, that was defined in 4, to the use conditions and the exploratory and extended stresses. Historical data (failure mechanisms & acceleration factors) and data obtained during the development of various BGA packages, along with the models from the previous section, were used to determine the exploratory and extended stresses shown in the Table C.

Table C
Exploratory and Extended Stresses/Conditions for PBGA Use Condition Qualification

Use Environment	Use Condition/Life	Proposed Stress	Exploratory Stress Conditions	Extended Stress conditions
Moisture Uptake in Mfg. Bd. Mount	1 week out of bag 220°C Reflow	Preconditioning	Level 3* JEDEC A113	Level 3* JEDEC A113
Slow small internal temp. changes due to external ambient	$\Delta T = 40^{\circ}C$ 3000 cycles	Temperature Cycle	-55/125°C 500 cyc. T/C “B”	-55/125°C 1500 cyc. T/C “B”
Fast, large internal temp. changes internally heated (on/off)	25°C to Tj max 7500 cycles	Power Cycle	25°C to Tj max 7500 cycles With thermal solution	25°C to Tj max 11K cycles With thermal solution
High Ambient Moisture during low-power state	30°C/85% RH 62K hrs	THB (HAST)	130°C/85% 50 hrs	130°C/85% 150 hrs
High Operating temperature Tj max	Tj max 62K hrs	Bake	150°C 500 hrs	150°C 1000 hrs 180°C ** 100 hrs
Storage Temperature	-40 to 55°C	Bake		

* Chosen application requirement for this example.

** Failures found using 180°C bake temperature should be carefully analyzed to insure they are relevant, since material properties at this temperature can be impacted.

6. Extended Stress Conditions

The exploratory and extended stresses defined in Table C are used to validate the activation energies, exponents and models selected. Parts should be stressed to a preselected failure percentage in order to verify the failure mechanism(s) that actually occur. The data from the extended stresses is also used to determine process margin and to make sure other failure mechanisms do not exist or are not relevant.

7. Apply Data to Models

Appendix B gives two examples of determining the activation energy or Coffin-Manson exponent from the data. The examples are graphical but the same information can be obtained mathematically. The graphical solution has the advantage that discontinuities in the data (e.g. two slopes) become readily apparent. Discontinuities would suggest that there is a new mechanism. This can result in inaccurate lifetime assessments.

The activation energies found are used to determine the acceleration factor of the chosen stress conditions in relation to the use condition. With the acceleration factor known you can easily determine the required time/cycles required to meet the use condition lifetime. You must be aware that the smallest activation energy or Coffin-Manson exponent found needs to be used to calculate the stress duration required.

Table D is a summary of the acceleration factors relating "USE" conditions to exploratory and extended stress conditions. They are derived from activation energies and exponents in Table B.

Table D
Acceleration Factors For Several Stress Conditions

			Acceleration Factors Use Condition vs. Stress Condition				
Rel Stress	Lifetime Requir.	Ea or CM exp	85°C /85%	HAST 130°C/85%	-40°C to 100°C DT=140°C	-55 to 125°C DT=180°C	BAK E 150°C
THB	62k hrs 30°C/85%	0.75 ev 0.91 ev	83 214	1254 5800			
Bake	62k hrs 100 °C	1.41 ev					180
Temp Cycle	3000 cy ΔT=40°C	1.25 2.2 3			4.8 15.7 43	6.6 27 91	

8. Determine Final Reliability Stress Conditions

Using the acceleration factors from Table D and the assumed use conditions and lifetimes, the reliability stress conditions and durations were determined. Table E shows the stresses and durations chosen. It also gives the equivalent life expected based on the use conditions and reliability stress chosen. In addition, Table E gives a comparison of what the equivalent life would be if the legacy qualification methodology were used.

Table E
Comparison of Use Condition to Legacy Qualification

Rel Stresses	Lifetime Requir.	Use Condition Qual		Legacy Qual		Data from Extended Stress	
		Stress Time/cycles	Equiv Life	Stress Time/cycles	Equiv Life	Stress Duration to 1% Fail	Actual Life To 1% Fail
THB	62k hrs 30°C/85%	85°C/85% 750 hrs 130°C/85% 50 hrs	62.2K hrs 62.7K hrs	85°C/85% 1000 hrs 130°C/85% 100 hrs	83K hrs 126K hrs	130°C/85% 148 hrs	187K hrs
Bake	62k hrs 100 °C	150 °C 500 hrs	90K hrs	150 °C 1000 hrs	180K hrs	180°C 96 hrs	225K hrs
Temp Cycle	3K cy ΔT=40 °C	T/C "B" 500 cyc	3.3K cyc	T/C "B" 1000 cyc	6.6K cyc	T/C "B" 1000 cyc	6.6K cyc

Note: JEDEC preconditioning performed prior to THB and TC stress

9. Establish Baseline Performance

In section 8, use condition qualification stress tests were performed, based on the application listed in section 4. These results must be analyzed to determine that the PBGA package meets or exceeds the application requirements, including end of life failure expectations. Test sample size versus test fails are important variables in failure rate determination. In particular, failure mechanisms must be reviewed to rule out: 1- fails that are not consistent with the field conditions and 2- fails that are relevant to the field, but occur beyond the end of life for the application. The latter can occur when failure mechanisms with a range of acceleration factors are present in the test samples. The failure mechanism with the highest acceleration factor should occur first. The test must be continued to discern if failure mechanisms with lower acceleration factors exist in that PBGA.

For this PBGA application, the last two columns of Table E relate the data obtained from the extended stresses to the actual life assuming 1% fail. This shows that for these packages that there is margin to the life at the assumed use conditions. It should be noted that if the legacy qualification requirements included 1000 cycles of TC "B" the device would have failed qualification and required design and/or material changes to pass, even though the component would meet the actual use condition requirements.

10. SUMMARY AND CONCLUSIONS

The paper has shown a specific example of how the use condition qualification methodology can be used. This approach is based on knowing the required lifetime of the package in its intended use and then performing qualification testing to meet the lifetime requirements. This also requires that the failure mechanisms and acceleration factors associated with each test be accurately determined. In this case, it was shown that qualification test times of approximately one-half to three-quarters of those associated with the legacy tests could be used to sufficiently qualify the package for its intended use. The advantages of using this methodology are potentially shorter qualification tests and a much more accurate prediction of lifetime performance, process margins and application specific failure rates.

APPENDIX A LEGACY TESTS

This table shows the typical (legacy) tests and ranges of test conditions presently used by member SEMATECH companies to qualify BGA packages. TABLE F was identified by the group as typical qualification tests versus BGA package type. Again the legacy thermal cycle test conditions are listed in this table.

LEGACY PACKAGE RELIABILITY STRESS TESTS

Preconditioning

JEDEC Levels 1-4 prior to Temp Cycle, Thermal Shock, Autoclave, and HAST

Autoclave (121°C, 2atm)

96-168 hours (45-105 parts)

HAST-with bias [130°C, 85% RH(33.3psia), 110°C, 85% RH(17.7psia)]

50- 264 hours (66-105 parts)

High Temperature Storage (150°C)

1000 hours (45-77 parts)

Temperature Cycle (air-to-air)

1000 cycles from 0°C to +100°C

3000 cycles from 0°C to +125°C

5 cycles from -40°C to +65°C (Ship Shock)

1000 cycles from -40°C to +115°C

1000 cycles from -40°C to +125°C

500-1000 cycles from -40°C to +150°C

500-1000 cycles from -55°C to +125°C (75-105 parts)

500 cycles from -65°C to +150°C (75-135 parts)

Thermal Shock (liquid-to-liquid)

10-500 cycles from -55°C / +125°C (25-231 parts)

THB (85°C, 85% RH with bias)

1000 hours (45-126 parts)

ESD

2kV HBM (15 parts)

1kV CDM (15 parts)

Bond Pull (3-20 parts)

Die Shear

Flammability (5 parts UL94VO S/O, UL1694 S/C O, U95VO)

Latch Up (5 parts)

Moisture Resistance (38 parts)

Solder Joint Reliability (1000 cycles from -40°C to +85°C)

Solvent Resistance (test done)

Variable Frequency Vibration (test done)

Coplanarity (15 parts)

Electrical Characterization (15 parts)

Mechanical Shock (test done)

Physical Dimensions (15 parts)

Salt Atmosphere (15 parts)

X-Ray (5-10 parts)

TABLE F: Thermal Cycle Test Conditions versus BGA Package Type From Member Company Input Consensus

TESTS	PBGA: Flip Chip	PBGA: WB	CBGA: Flip Chip	CBGA: WB	TBGA: Flip Chip	TBGA: WB
THERMAL CYCLING*	1,2,3,5,6,8	2,3,5,6,8	1,2,3,5,8	2,3,5,8	1,2,3,5,6,8	2,3,5,6,8
SHIP SHOCK -40C TO 65C	9	9	9	9	9	9
THERMAL CYCLING* with JEDEC Precondition & Assembly	4,7	4,7	4,7	4,7	4,7	4,7
Wet TC (Thermal Shock or Deep TC -55 to 125C	10	10	10	10	10	10
POWER CYCLING	Option for T/C	Same	Same	Same	Same	Same
HAST	Alt. Test for Delamin	Same	Same	Same	Same	Same

FAILURE MECHANISM of INTEREST

- 1: CTE Mismatch Device to Package
- 2: CTE Mismatch Module to PWB
- 3: CTE Mismatch Encapsulant to Device
- 4: Delamination and Loss of Adhesion at Interfaces
- 5: Solder Creep Rupture
- 6: Metal Circuit Fatigue
- 7: Assembly Induced Problems
- 8: Defect Failures
- 9: Device Cracking
- 10: Passivation/Thin Film Cracking

* Select Appropriate Thermal Cycle Range and Duration. Test selection, even as a legacy test, must be selected based on use environment. Selection of extreme test conditions can result in test failures not representative of the field.

Appendix B

Examples of Finding Acceleration Factors, Activation Energy and Coffin-Manson Exponent

Figure 1 is a Weibull plot of temperature cycle data taken on two different die sizes. Two conditions of TC were used so the effects of die size and ΔT could be evaluated. The plot shows the acceleration factor to be 2.3 for the TC condition. Using the Coffin-Manson model from 4 and solving for the exponent "n" using $AF = 2.3$, $\Delta T_S = 165^\circ\text{C}$ and $\Delta T_{USE} = 100$ we find a Coffin-Manson exponent "n" of 1.64

$$AF = \left[\frac{\Delta T_{Stress}}{\Delta T_{Use}} \right]^n$$

$$n = \frac{\text{Ln} (AF)}{\text{Ln} \left(\frac{\Delta T_S}{\Delta T_{Use}} \right)}$$

Best Fit
 n=1.64

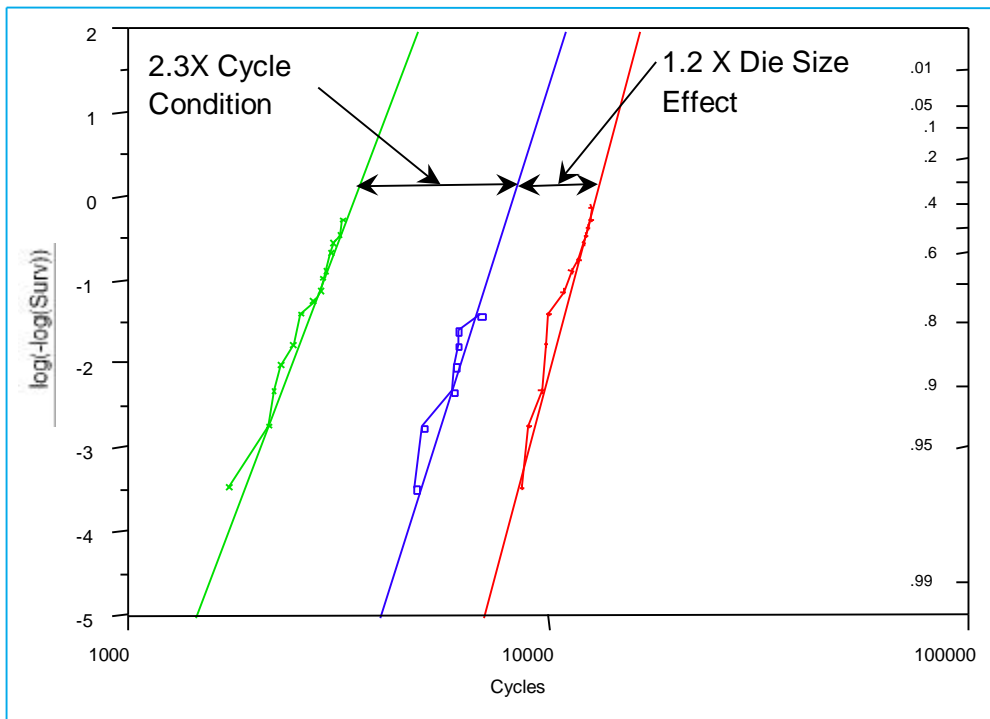


Figure 1
Temperature Cycle 2 die sizes and 2 TC Conditions
-40C/125C & 0C/100C

Figure 2 is an Arrhenius plot of time to 10% wire pull fail versus bake temperature. The slope of the curve is the activation energy. We can also obtain the activation energy by determining the acceleration factor and using this in the Arrhenius equation after solving for E_A . From the plot we determine the $AF = 533$ from 180°C to 300°C (453°K to 573°K). Using these numbers in the equation for E_A below we find the activation energy to be 1.17 eV. This E_A can now be used to calculate the acceleration factor (AF) between any use/stress condition.

$$AF = e^{\frac{E_A}{k} \left(\frac{1}{T_1} - \frac{1}{T_2} \right)}$$

$$E_A = \frac{T_1 T_2 k (\ln(AF))}{T_2 - T_1}$$

$E_A = 1.17$

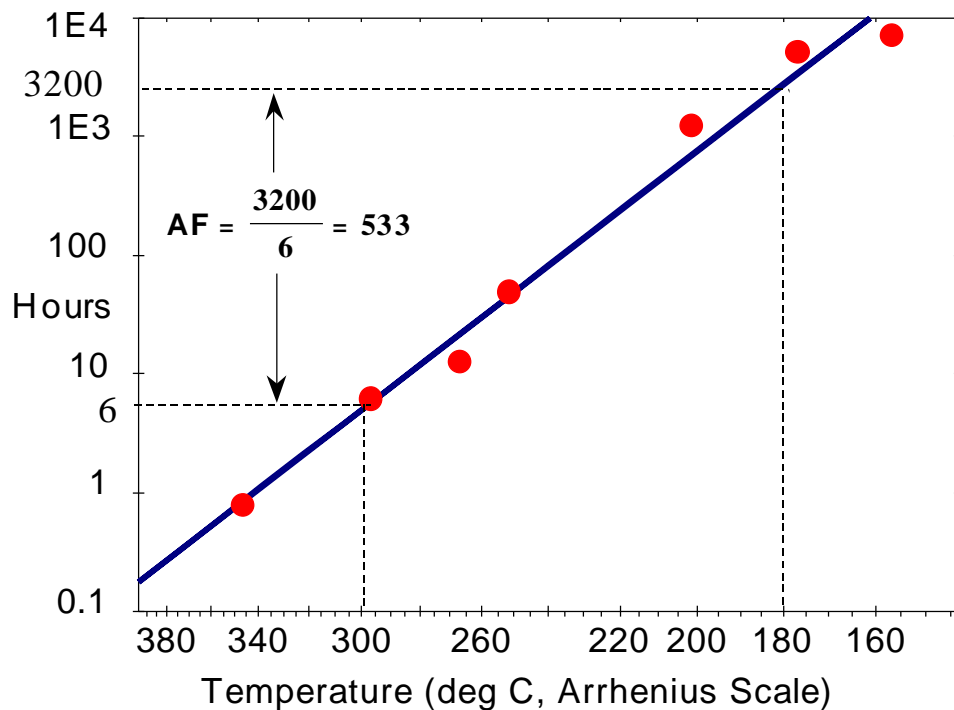


Figure 2
Arrhenius Plot of Time to 10% wire pull fail

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